OCP SUMMIT

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San Jose, CA

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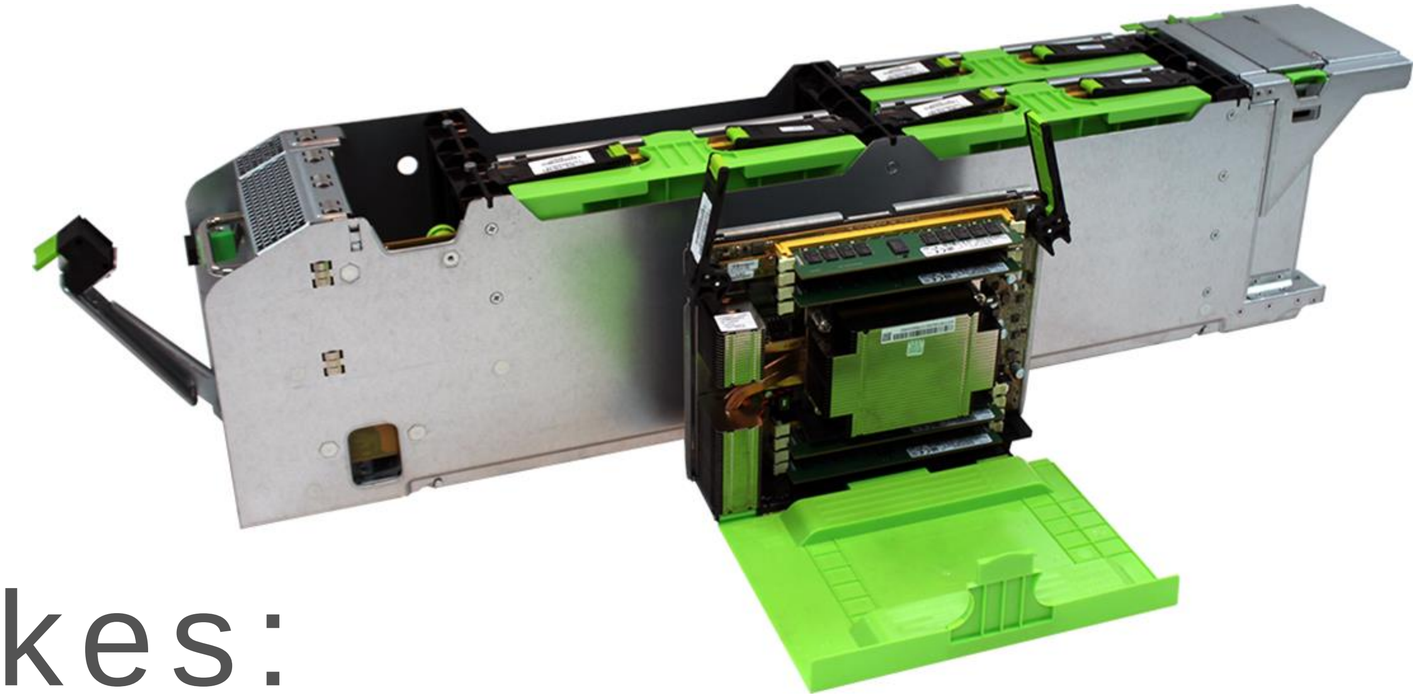
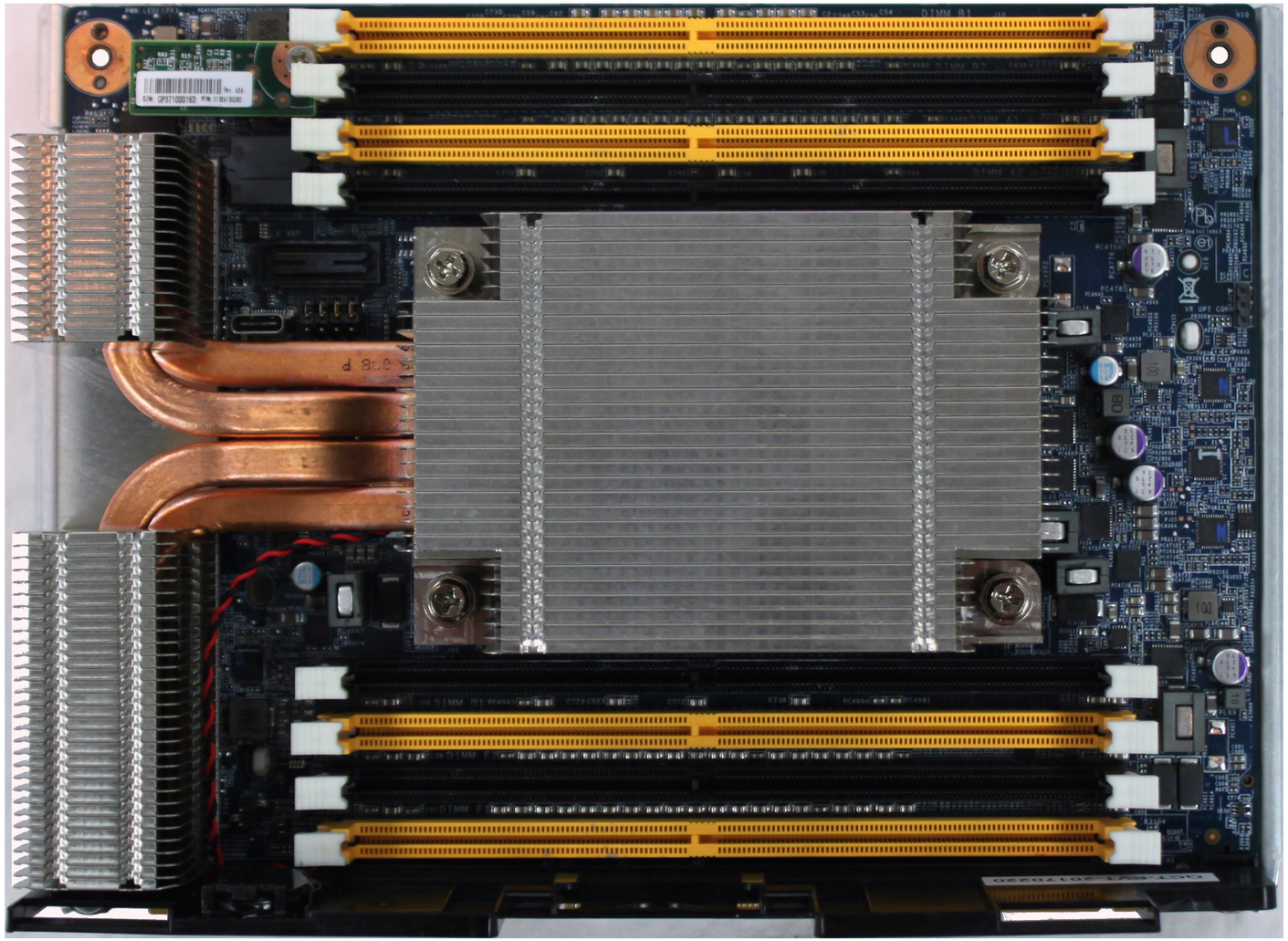


Twin Lakes: 1S Server for Yosemite V2

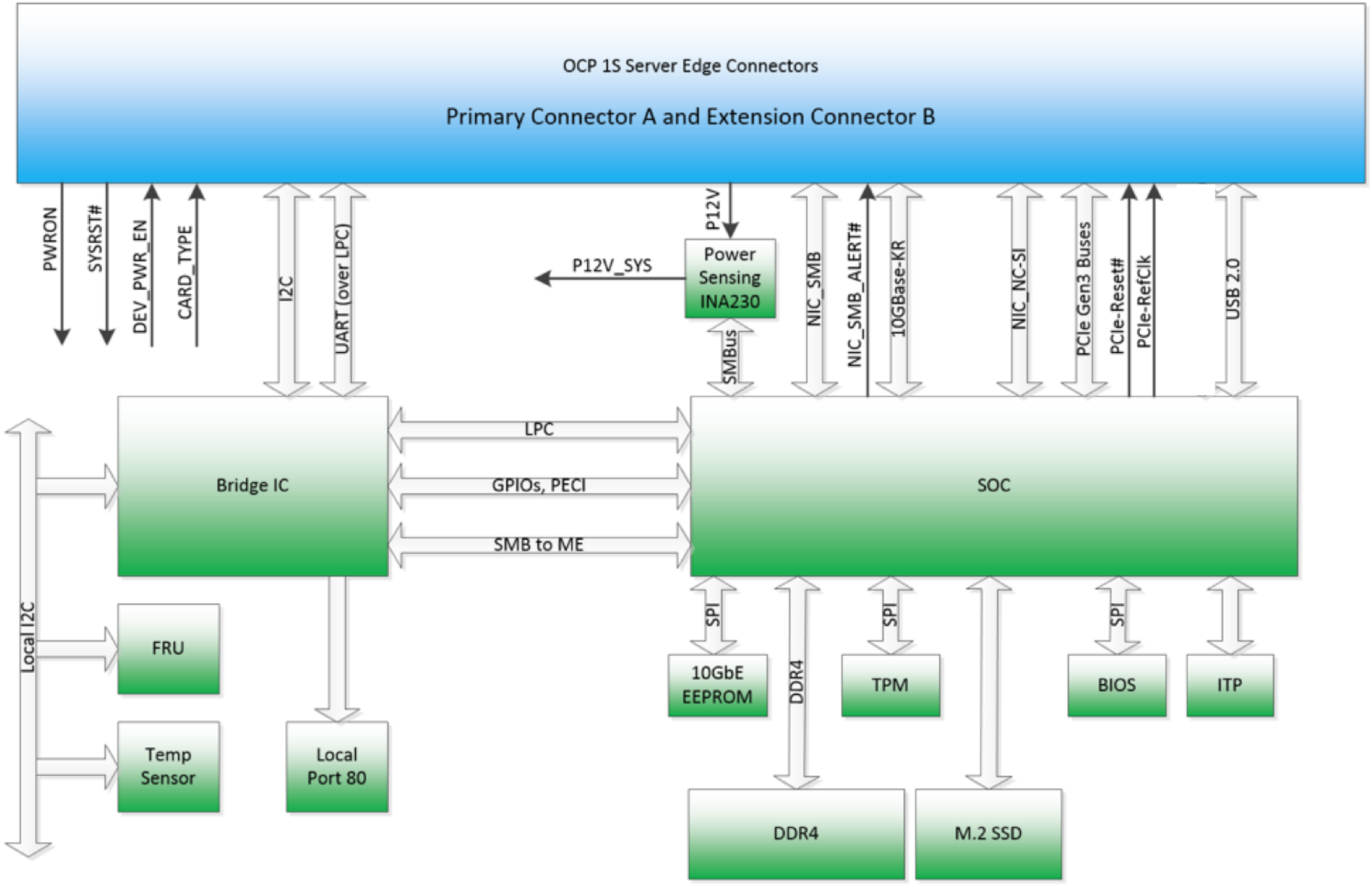
John Bryan, Platform Architect, Intel

Damien Chong, Hardware Engineer, Facebook



Twin Lakes Server for Yosemite V2:

- Intel® Xeon® D-2100 Processor
- Eight RDIMM Sockets
- 32+ PCIe Lanes
- 3 Local M.2
- Flexible Networking
- Trusted Boot



Twin Lakes is architected to support dense I/O and high manageability

	Intel® Xeon® D-2100 Processor	Intel® Xeon® D-1500 Processor
CPU Cores	Up to 18 with Intel® HT	Up to 16 with Intel® HT
Cache	LLC: 1.375 MB/Core MLC: 1 MB/Core	LLC: 1.5 MB/Core MLC: 256 KB/Core
Memory	4 Channels, DDR4 1866/2133/2400/2667*	2 Channels DDR4/DDR3L 1600/1866/2133
PCIe	CPU: x32 PCIe Gen 3 • Twin Lakes uses all 32 lanes FlexIO: x20 PCIe Gen 3 • Twin Lakes uses 9 FlexIO PCIe lanes	CPU: x24 PCIe Gen 3 lanes FlexIO: x8 PCIe Gen 2 lanes
Acceleration Engines	AVX512 Intel® QuickAssist Technology* • Up to 100 Gbps Crypto/Compression • 100 KOps PKE 2K	AVX256 No built-in Intel® QAT

* Intel® Xeon® D-2100 Processor feature not validated on the Twin Lakes 1S Server

Twin Lakes is architected for high compute performance

Learn More About Twin Lakes

- Twin Lakes OCP Specification:
  http://www.opencompute.org/products/specsanddesign?keyword=twin+lakes
- Twin Lakes Blog:
  https://itpeernetwork.intel.com/
- Visit the Intel Booth to see Twin Lakes in action

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